

CLAIMS:

1           1.    A method of engaging electrically conductive test pads on  
2   a semiconductor substrate having integrated circuitry for operability  
3   testing thereof, the method comprising the following sequential steps:

4           providing an engagement probe having an outer surface comprising  
5   a grouping of a plurality of electrically conductive projecting apices  
6   positioned in proximity to one another to engage a single test pad on  
7   a semiconductor substrate;

8           engaging the grouping of apices with the single test pad on the  
9   semiconductor substrate; and

10          sending an electric signal between the grouping of apices and test  
11   pad to evaluate operability of integrated circuitry on the semiconductor  
12   substrate.

1           2.    The method of engaging electrically conductive test pads of  
2   claim 1 wherein the step of engaging comprises pressing the grouping  
3   of apices against the single test pad sufficiently to penetrate the apices  
4   into the test pad.

3. The method of engaging electrically conductive test pads of claim 1 wherein the step of engaging comprises pressing the grouping of apexes against the single test pad sufficiently to penetrate the apexes into the test pad a distance of only about one-half the test pad thickness.

4. A method of forming a testing apparatus for engaging electrically conductive test pads on a semiconductor substrate having integrated circuitry for operability testing thereof, the method comprising the following steps:

providing a locally substantially planar outer surface of a first material on a semiconductor substrate;

providing a layer of second material atop the substantially planar outer surface of first material, the second material being capable of substantially masking the underlying first material;

patterning and etching the layer of second material to selectively outwardly expose the first material and define a grouping of discrete first material masking blocks, the discrete first material masking blocks of the grouping having respective centers, the respective centers of the grouping being positioned in sufficient proximity to one another such that the centers of the grouping fall within confines of a given single test pad which the apparatus is adapted to electrically engage;

forming projecting apexes beneath the masking blocks at the masking block centers, the projecting apexes forming a group falling

19 within the confines of the given single test pad of which the apparatus  
20 is adapted to electrically engage;

21 removing the discrete first material masking blocks from the  
22 substrate after the exposing step; and

23 rendering the projecting apexes electrically conductive.

1 5. The method of forming a testing apparatus of claim 4  
2 wherein the second material is capable of substantially masking the  
3 underlying first material from oxidation when the semiconductor substrate  
4 is exposed to oxidizing conditions, the step of forming the projecting  
5 apexes comprises:

6 exposing the semiconductor substrate to oxidizing conditions  
7 effective to oxidize the exposed outer surface of first material and  
8 oxidize first material beneath the masking blocks to form the projecting  
9 apexes at the masking block centers, and further comprising stripping  
10 oxidized first material from the substrate.

1 6. The method of forming a testing apparatus of claim 5  
2 wherein the steps of exposing and stripping comprise multiple exposing  
3 and stripping steps.

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1           7.    The method of forming a testing apparatus of claim 5  
2    wherein the first material predominately comprises silicon, and the  
3    second material predominately comprises a nitride.

1           8.    The method of forming a testing apparatus of claim 4  
2    wherein the layer of second material is provided to a thickness of from  
3    about 500 Angstroms to about 3000 Angstroms.

1           9.    The method of forming a testing apparatus of claim 4  
2    wherein the steps of patterning and etching and forming comprise  
3    forming multiple groupings of discrete masking blocks and multiple  
4    groups of projecting apexes, each group being sized and configured for  
5    engaging a respective single test pad.

1           10.   The method of forming a testing apparatus of claim 4  
2    wherein the steps of patterning and etching and forming produce  
3    projecting apexes in the form of multiple knife-edge lines.

1           11.   The method of forming a testing apparatus of claim 4  
2    wherein the steps of patterning and etching and forming produce  
3    projecting apexes in the form of multiple knife-edge lines, the multiple  
4    knife-edge lines interconnecting to form at least one polygon.

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1 12. The method of forming a testing apparatus of claim 4  
2 wherein the steps of patterning and etching and forming produce  
3 projecting apexes in the form of multiple knife-edge lines, the multiple  
4 knife-edge lines interconnecting to form at least two polygons one of  
5 which is received entirely within the other.

1 13. The method of forming a testing apparatus of claim 4  
2 wherein the apexes have a selected projecting distance, the projecting  
3 distance being about one-half the thickness of the test pad which the  
4 apparatus is adapted to engage.

1 14. The method of forming a testing apparatus of claim 4  
2 wherein the steps of patterning and etching and forming produce apexes  
3 which project from a common plane, the apexes having respective tips  
4 and bases, the bases of adjacent projecting apexes being spaced from  
5 one another to define a penetration stop plane therebetween.

15. The method of forming a testing apparatus of claim 4 wherein the steps of patterning and etching and forming produce apexes which project from a common plane, the apexes having respective tips and bases, the bases of adjacent projecting apexes being spaced from one another to define a penetration stop plane therebetween, the tips being a distance from the penetration stop plane of about one-half the thickness of the test pad which the apparatus is adapted to engage.

16. The method of forming a testing apparatus of claim 4 further comprising masking the projecting apexes and etching into the substrate around the masked projecting apexes to form a projection outwardly of which the projecting apexes project.

17. The method of forming a testing apparatus of claim 4 wherein the step of rendering comprises:

providing and patterning photoresist to outwardly expose the projecting apexes, selected area adjacent thereto, and cover selected remaining portions of the substrate;

applying a current to the substrate and electroplating a metal on the substrate onto the outwardly exposed projecting apexes and adjacent area; and

stripping photoresist from the substrate.

18. The method of forming a testing apparatus of claim 17 further comprising:

depositing an electrically conductive nucleation layer atop the apexes and substrate prior to providing and patterning the photoresist; the step of providing and patterning photoresist comprising outwardly exposing the nucleation layer coated projecting apexes, selected nucleation layer coated area adjacent thereto, and cover selected remaining nucleation layer coated portions of the substrate;

the step of applying current to the substrate comprising applying current to the nucleation layer and electroplating the metal onto the outwardly exposed nucleation layer coated projecting apexes and outwardly exposed nucleation layer coated adjacent area;

stripping photoresist from the substrate; and

stripping nucleation layer material from the substrate selectively relative to the metal.

19. The method of forming a testing apparatus of claim 17 further comprising:

depositing an electrically conductive nucleation layer atop the apexes and substrate prior to providing and patterning the photoresist;

the step of providing and patterning photoresist comprising outwardly exposing the nucleation layer coated projecting apexes, selected nucleation layer coated area adjacent thereto, and cover selected remaining nucleation layer coated portions of the substrate;

the step of applying current to the substrate comprising applying current to the nucleation layer and electroplating the metal onto the outwardly exposed nucleation layer coated projecting apexes and outwardly exposed nucleation layer coated adjacent area;

stripping photoresist from the substrate;

stripping nucleation layer material from the substrate selectively relative to the metal; and

after stripping nucleation layer material from the substrate selectively relative to the metal, applying another dose of current to the nucleation layer to electroplate another metal on top of the metal.



1           20. The method of forming a testing apparatus of claim 17  
2 further comprising:

3           prior to providing and patterning photoresist, providing an  
4 insulating layer over the substrate and projecting apexes;

5           after providing the insulating layer over the substrate but still  
6 prior to providing and patterning photoresist, depositing an electrically  
7 conductive nucleation layer atop the apexes;

8           the step of providing and patterning photoresist comprising  
9 outwardly exposing the insulating layer and nucleation layer coated  
10 projecting apexes, selected nucleation layer exposed area adjacent  
11 thereto, and cover selected remaining nucleation layer coated portions  
12 of the substrate;

13          the step of applying current to the substrate comprising applying  
14 current to the nucleation layer and electroplating the metal onto the  
15 outwardly exposed nucleation layer coated projecting apexes and  
16 outwardly exposed nucleation layer coated adjacent area;

17          stripping photoresist from the substrate; and

18          stripping nucleation layer material from the substrate selectively  
19 relative to the metal.

1 21. A testing apparatus for engaging electrically conductive test  
2 pads on a semiconductor substrate having integrated circuitry for  
3 operability testing thereof, the apparatus comprising:

4 a test substrate; and

5 an engagement probe projecting from the test substrate to engage  
6 a single test pad on a semiconductor substrate having integrated  
7 circuitry formed in the semiconductor substrate, the engagement probe  
8 having an outer surface comprising a grouping of a plurality of  
9 electrically conductive projecting apexes positioned in sufficient proximity  
10 to one another to collectively engage the single test pad.

1 22. The testing apparatus of claim 21 comprising a plurality of  
2 such engagement probes.

1 23. The testing apparatus of claim 21 wherein the apexes are  
2 in the shape of multiple knife-edge lines.

1 24. The testing apparatus of claim 21 wherein the apexes are  
2 in the shape of multiple knife-edge lines, the multiple knife-edge lines  
3 interconnecting to form at least one polygon.

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1 25. The testing apparatus of claim 21 wherein the apexes are  
2 in the shape of multiple knife-edge lines, the multiple knife-edge lines  
3 interconnecting to form at least two polygons one of which is received  
4 entirely within the other.

1 26. The testing apparatus of claim 21 wherein the engagement  
2 probe is formed on a projection from the substrate.

1 27. The testing apparatus of claim 21 wherein the apexes have  
2 a selected projecting distance, the projecting distance being about  
3 one-half the thickness of the test pad which the apparatus is adapted  
4 to engage.

1 28. The testing apparatus of claim 21 wherein the apexes have  
2 a selected projecting distance, the projecting distance being about  
3 one-half the thickness of the test pad which the apparatus is adapted  
4 to engage.

1 29. The testing apparatus of claim 21 wherein the apexes  
2 project from a common plane, the apexes having respective tips and  
3 bases, the bases of adjacent projecting apexes being spaced from one  
4 another to define a penetration stop plane therebetween.

1 30. The testing apparatus of claim 21 wherein the apexes  
2 project from a common plane, the apexes having respective tips and  
3 bases, the bases of adjacent projecting apexes being spaced from one  
4 another to define a penetration stop plane therebetween, the tips being  
5 a distance from the penetration stop plane of about one-half the  
6 thickness of the test pad which the apparatus is adapted to engage.

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